uN8130
GPS Baseband Processor

Features

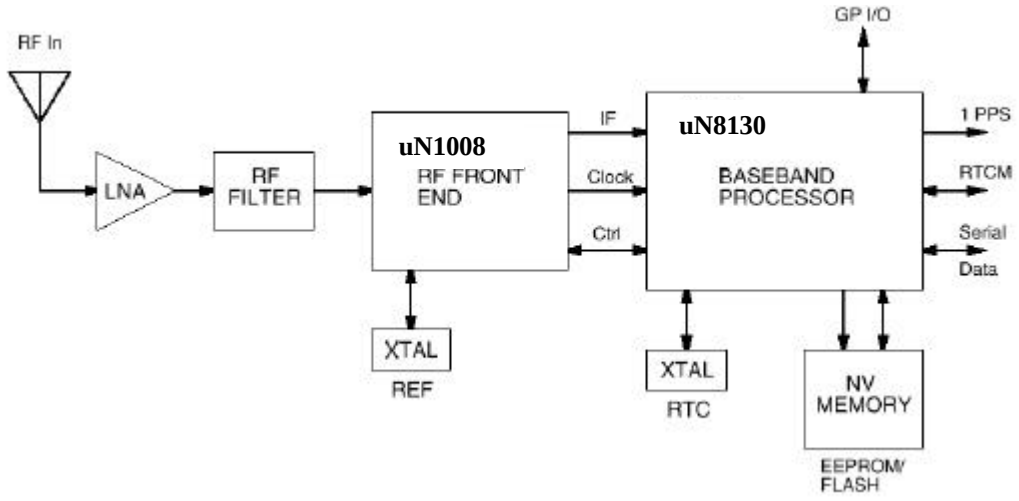
- Modular and scalable ASiS™ (Application Specific Integrated System) architecture in CMOS technology
- Ideally suited for embedded portable applications
- 12 channel parallel receiver with programmable Zoom Correlators™
- Fast signal acquisition with dedicated QwikLock™ search engine supporting up to four frequency bins simultaneously
- Integrated low-power 16-bit proprietary VS_ DSP core with barrel shifter and instructions for fast FFT
- On-chip SRAM memories
- 1.8V or 3V I/O and 1.8V core power supplies
- Low power consumption enabled by PowerMiser™
- Small Form Factor – 10x10x1.4 mm^3 144-pin BGA, 7x7x1.4mm^3 121-pin BGA, and 7x7x1.4mm^3 BGA 49 package, and 5x5x0.65 mm^3 WLP package
- Glueless interface to external u-Nav uN802x RF and uN100x front-ends
- Input master clock frequency doubler
- MultMediaCard™ (MMC) controller, master and slave SPI, IrDA interface, and extensive timers including watchdog

Description

This second generation u-Nav Microelectronics GPS baseband processor uN8130 is the successor to the uN8031 and features enhanced search engine, extended DSP instruction set, and expanded peripherals including MMC flash storage module support, asynchronous serial IrDA interface to 115.2kbps, and extensive timer resources. The uN8130 Wafer Level Packaged *WLP* is functionally identical to the uN8130 BGA package versions and includes all baseband functions needed for GPS signal acquisition, tracking and navigation. A dedicated high-performance search engine using patented QwikLock™ architecture enables a rapid search of visible satellites. An advanced tracking unit employing twelve Zoom Correlators™ insures that positioning is possible even in severe conditions such as in urban canyons and under foliage.

A complete GPS receiver built with a uN8130 baseband IC and a uN802x or uN100x RF front-end IC needs only a handful of external components, keeping the overall bill of materials to a minimum. A typical application diagram is shown below.

Figure 1. GPS Receiver Based on u-Nav Chip Set



Final Data Sheet

Doc. No. 813002 June 23, 2006

Block Diagram

The uN8130 block diagram is shown below:

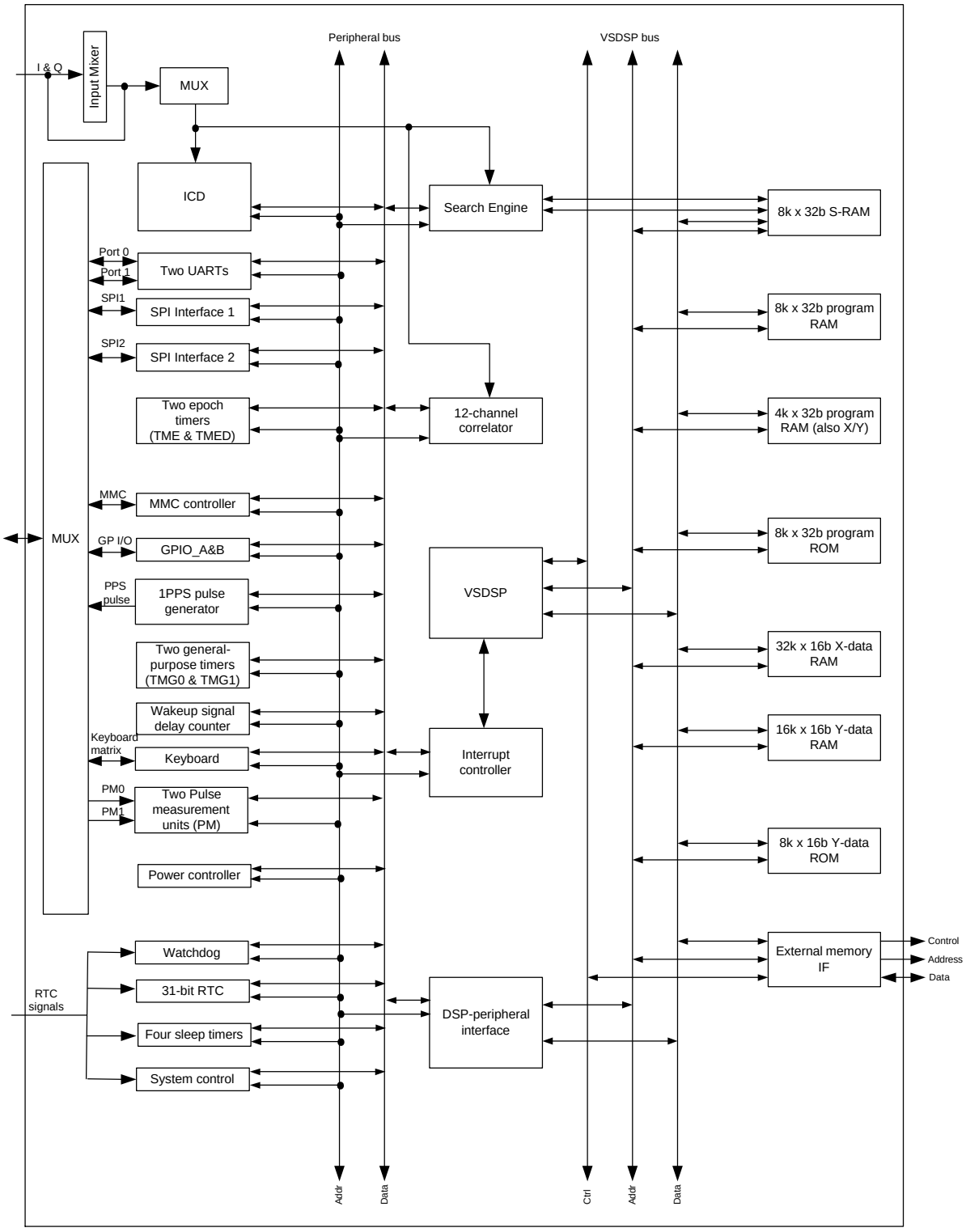


Figure 2. uN8130 Block Diagram

Pin Description

The pin description for the uN8130 defined for the BGA-49, BGA-121, and BGA-144 and WLP packages is defined in Table 1 below. BGA ball-out is defined in tables 2 and 5 respectively while WLP pad location is given in the packaging section. The pin functionality only available in the BGA 144, 121, and WLP package option is denoted in the package column as "*144/121/WLP*". Functionality available in all package options is denoted "*all*". Pin types are digital "*I/O*", digital "*In*", digital "*Out*", "Power", and "Analog". Multifunction pin type is listed matching multifunction pin primary/secondary order.

Group	Name	Type	Package	Description
External Bus	D[15..0]	I/O	144/121/WLP	External data bus.
	A[19..0]	Out	144/121/WLP	External address bus.
	XCS[3..0]	Out	144/121/WLP	Active low chip select outputs.
	XWT	In	144/121/WLP	Active low asynchronous wait state request for external bus. Can be left unconnected when not used.
	XWR	Out	144/121/WLP	Active low write strobe for external bus.
	XRD	Out	144/121/WLP	Active low read strobe for external bus.
Control	MCLK	In	All	Master clock input nominally 16.x MHz
	XRESET	In	All	Active low asynchronous system reset input.
	RF_EN/GPIO_B23	Out	144/121/WLP	Active-high enable/power-down signal to external RF front-end
	RF_XEN/GPIO_B24	Out	144/121/WLP	Active-low enable/power-down signal to external RF front-end
	RF_EN/GPIO_B25	Out	All	Active-high enable/power-down signal to external RF front-end
	RF_XEN/GPIO_B26	Out	All	Active-low enable/power-down signal to external RF front-end

Real time clock	RTC_XIN	Analog In	All	RTC (Real Time Clock) XTAL oscillator input pin (32768 Hz).
	RTC_XOUT	Analog Out	All	RTC XTAL oscillator output pin (32768 Hz).
RF Front-end	ISIGN	In	All	In-phase arm IF signal sign input
	IMAGN	In	All	In-phase arm IF signal magnitude input
	QSIGN	In	All	Quadrature arm IF signal sign input
	QMAGN	In	All	Quadrature arm IF signal magnitude input
SPI Interface	SPI1_CLK	Out	144/121/WLP	Serial clock output for devices connected to SPI1
	SPI1_SDO	Out	144/121/WLP	Serial data output to devices connected to SPI1
	GPIO_B10/SPI1_XCS0	I/O; Out	All	Chip select for separate device #0 on SPI1
	GPIO_B11/SPI1_XCS1	I/O; Out	All	Chip select for separate device #1 on SPI1
	GPIO_B12/SPI1_XCS2	I/O; Out	All	Chip select for separate device #2 on SPI1
	SPI1_XCS3	Out	144/121/WLP	Chip select for separate device #3 on SPI1
	GPIO_B13/SPI1_CLK	I/O; Out	All	Alternate serial clock output for devices connected to SPI1
	GPIO_B14/SPI1_SDO	I/O; Out	All	Alternate data output to devices connected to SPI1
	GPIO_B15/SPI1_SDI	I/O; In	All	Serial data input from devices connected to SPI1
	GPIO_B16/SPI2_CLK	I/O; Out	144/121/WLP	Serial clock output for devices connected to SPI2

	GPIO_B17/SPI2_SDO	I/O; Out	All	Serial data output for devices connected to SPI2
	GPIO_B18/SPI2_SDI	I/O; In	All	Serial data input from devices connected to SPI2
	GPIO_B19/SPI2_XCS0	I/O; Out	144/121/WLP	Chip select for separate device #0 on SPI2
	GPIO_B20/SPI2_XCS1	I/O; Out	144/121/WLP	Chip select for separate device #1 on SPI2
	GPIO_B21/SPI2_XCS2	I/O; Out	All	Chip select for separate device #2 on SPI2
	GPIO_B22/SPI2_XCS3	I/O; Out	144/121/WLP	Chip select for separate device #3 on SPI2
Peripherals	GPIO_B0/KBDOUT0	I/O; Out	144/121/WLP	Keyboard controller row #0 select output
	GPIO_B1/KBDOUT1	I/O; Out	144/121/WLP	Keyboard controller row #1 select output
	GPIO_B2/KBDOUT2	I/O; Out	144/121/WLP	Keyboard controller row #2 select output
	GPIO_B3/KBDOUT3	I/O; Out	144/121/WLP	Keyboard controller row #3 select output
	GPIO_B4/KBDOUT4	I/O; Out	All	Keyboard controller row #4 select output
	GPIO_B5/KBDIN0	I/O; In	All	Keyboard controller column #0 input. Can be left NC when not used
	GPIO_B6/KBDIN1	I/O; In	All	Keyboard controller column #1 input. Can be left NC when not used
	GPIO_B7/KBDIN2	I/O; In	All	Keyboard controller column #2 input. Can be left NC when not used
	GPIO_B8/KBDIN3	I/O; In	All	Keyboard controller column #3 input. Can be left NC when not used

	GPIO_B9/KBDIN4	I/O; In	All	Keyboard controller column #4 input. Can be left NC when not used
	GPIO_A0/RXD0	I/O; In	All	CMOS level asynchronous input for UART port #0. Can be left NC when not used
	GPIO_A1/TXD0	I/O; Out	All	CMOS level asynchronous output for UART port #0
	GPIO_A2/RXD1	I/O; In	All	CMOS level asynchronous input for UART port #1. Can be left NC when not used
	GPIO_A3/TXD1	I/O; Out	All	CMOS level asynchronous output for UART port #1
	GPIO_A4/FCLK	I/O; Out	144/121/WLP	Pre-divided clock output of UART port #1
	GPIO_A5/PM0	I/O; In	All	Input for pulse measurement 0. Can be left NC when not used
	GPIO_A6/PM1	I/O; In	144/121/WLP	Input for pulse measurement 1. Can be left NC when not used
	GPIO_A7/PPS	I/O; Out	All	1PPS signal output
	GPIO_A8/TIN0	I/O; In	144/121/WLP	Timer TMG0 external clock input
	GPIO_A9/TCAP0	I/O; In	144/121/WLP	Timer TMG0 capture input
	GPIO_A10/TIN1	I/O; In	All	Timer TMG1 external clock input
	GPIO_A11/TCAP1	I/O; In	All	Timer TMG1 capture input
	GPIO_A12/MMC_CLK	I/O; Out	All	MultiMediaCard interface clock output
	GPIO_A13/MMC_CMD	I/O; I/O	All	MultiMediaCard interface command bus

	GPIO_A14/MMC_DATA	I/O; I/O	All	MultiMediaCard interface data bus
Test	TEST	In	All	Active high test mode select input. Connect to GND for normal operation. Other test pins are shared with GPIO.
Power pins	DVDD	Power	All	Core power
	XVDD	Power	All	PLL power
	IOVDD	Power	All	Peripheral I/O device interface power, 3V or 1.8V
	GND	Power	All	Pad and core control

Table 1. uN8130 Pin Description

The uN8130 has three different power supply pins identified below:

Name	Description
DVDD	Digital core, nominally 1.8V
XVDD	PLL power, nominally 1.8V
IOVDD	All GPIO, external bus, and other digital interface signal pins; 3V or 1.8V

Table 2. uN8130 Power Supply Pins

XVDD should be at the same voltage level as DVDD. XVDD should be additionally filtered from DVDD to minimize noise coupling into PLL. IOVDD supports 3V or 1.8V I/O CMOS logic levels; all pins must operate at the same level, mixed 3V and 1.8V I/O is not supported.

Some of the interfaces of *uN8130* include internal a pull-up resistor, pull-down resistor, or keeper; therefore no external resistor is required if the pin is left not connected. GPIO pins have configurable input type and unused pins should be programmed to be something other than floating. For SPI SDI pins, program resistive pull-up. Note that internal resistors or keeper is not intended to drive external loads; these straps are applicable only to the internal input receiver. Further, the internal strap level may not be observable externally due to the I/O pad construction. The following table lists these special pins:

Pin	Type
GPIO_A[14..0], GPIO_B[26..0]	Configurable keeper, 50kΩ pull-down, 74kΩ pull-up, or floating
XWT	74kΩ pull-up

Table 3. Special Input Pin Types

Package Description

uN8130 has four packing options: uN8130-B144 for BGA-144, uN8130-B121 for BGA-121, uN8130-WLP, and uN8130-B49 for BGA-49 packages. BGA-144, BGA-121, and WLP packages offer full external memory bus and full I/O device connectivity, while BGA-49 offers a minimum footprint and a minimum amount of interface devices. See the WLP Package Information section for pad location information for the WLP package.

The BGA-49 package dimensions (in millimeters) and ball identifiers are as shown in the outline drawing below:

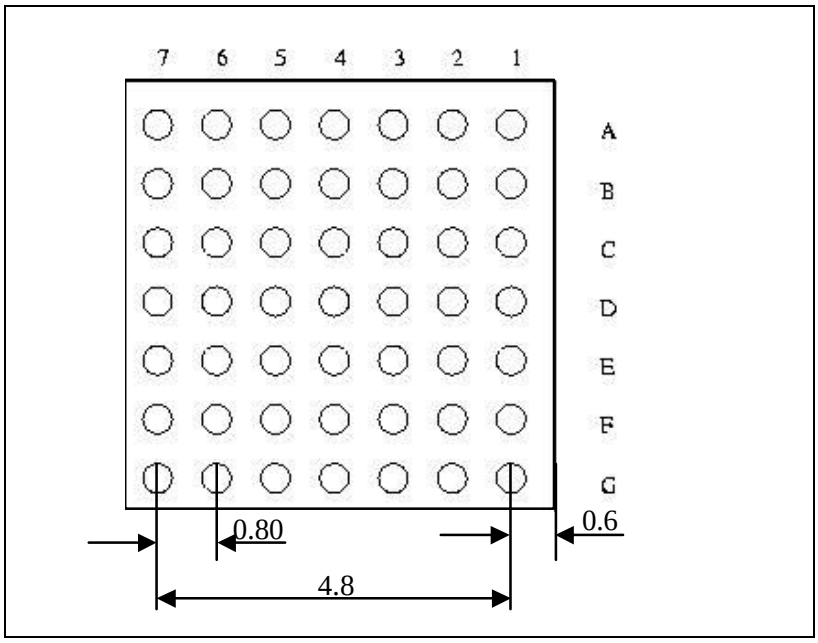


Figure 3. uN8130-B49 Package Outline

The BGA-144 package dimensions (in millimeters) and ball identifiers are as shown in the outline drawing below:

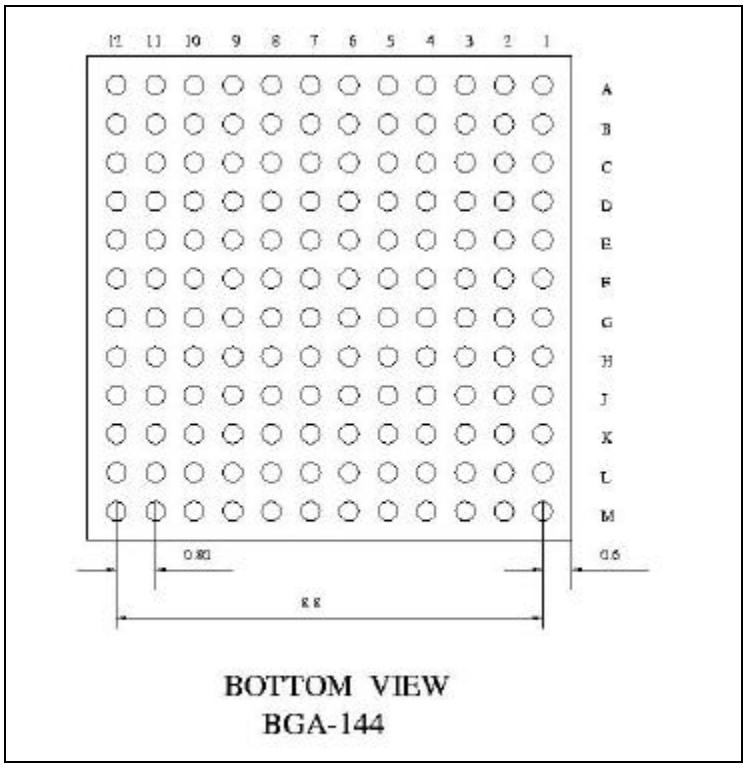


Figure 4. uN8130-B144 Package Outline

The BGA-121 package dimensions (in millimeters) and ball identifiers are as shown in the outline drawing below:

Contact u-Nav Applications for this information

Figure 5. uN8130-B121 Package Outline

WLP package information is shown below:

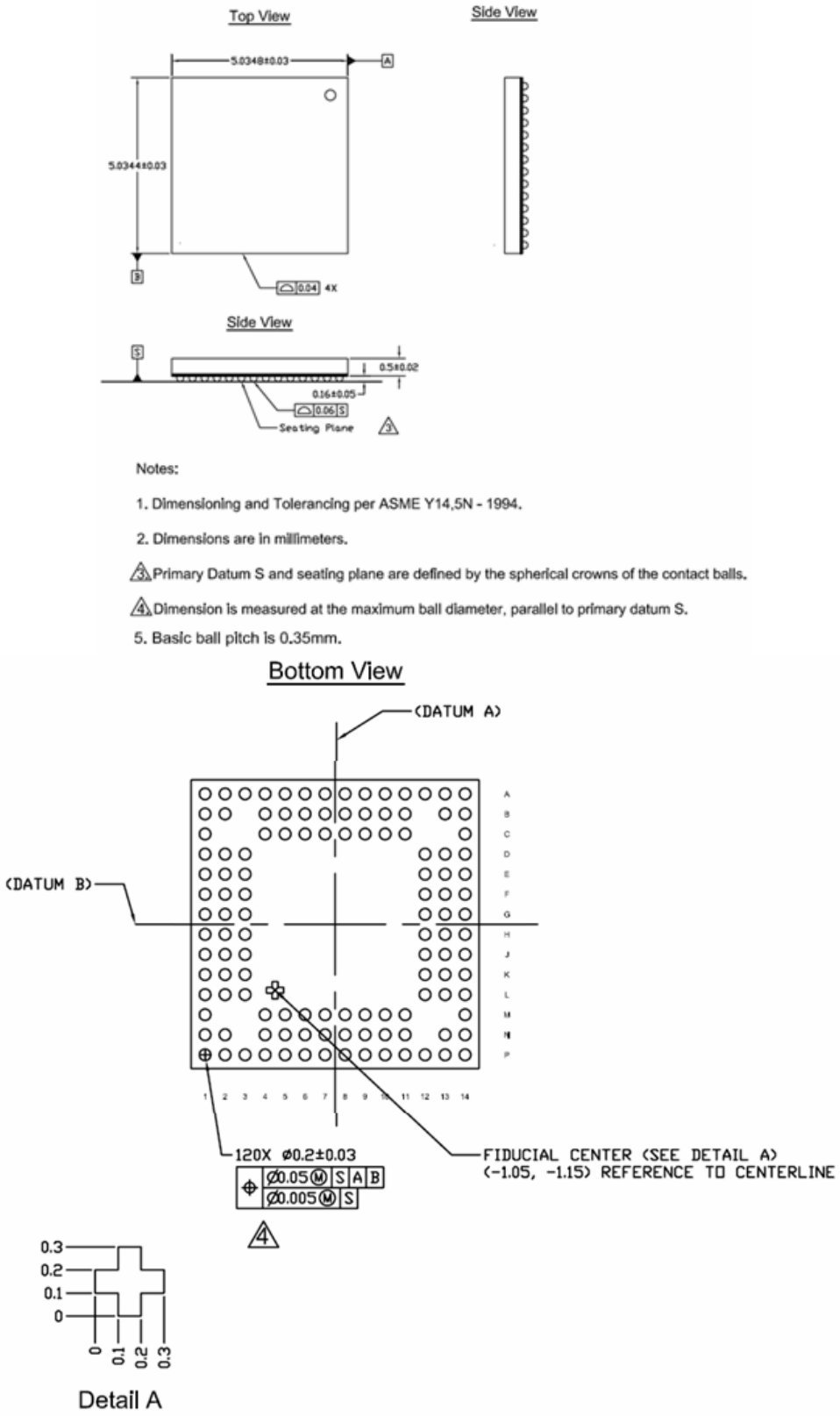


Figure 6. uN8130 WLP Package Outline

Ball-Out Description

The ball-out for the B49 package option is listed in the table below:

Ball	Name	Ball	Name
A1	QMAGN	E1	GPIO_B21/ SPI2_XCS2
A2	QSIGN	E2	GPIO_B13/SPI1_CLK
A3	RTC_XOUT	E3	DVDD
A4	RTC_XIN	E4	GND
A5	GPIO_B15/SPI1_SDI	E5	GND
A6	GPIO_B10/SPI1_XCS0	E6	GPIO_A14/MMC_DATA
A7	GPIO_B7/KBDIN2	E7	GPIO_A11/TCAP1
B1	IMAGN	F1	GPIO_B17/SPI2_SDO
B2	ISIGN	F2	GPIO_B12/SPI1_XCS2
B3	XRESET	F3	GPIO_B6/KBDIN1
B4	GPIO_B18/SPI2_SDI	F4	IOVDD
B5	GPIO_B14/SPI1_SDO	F5	GPIO_A3/TXD1
B6	GPIO_B11/SPI1_XCS1	F6	GPIO_A7/PPS
B7	GPIO_B8/KBDIN3	F7	GPIO_A5/PM0
C1	MCLK	G1	GPIO_B9/KBDIN4
C2	RF_EN/GPIO_B25	G2	GPIO_A13/MMC_CMD
C3	XVDD	G3	GPIO_A12/MMC_CLK
C4	GND	G4	GPIO_A1/TXD0
C5	DVDD	G5	GPIO_A0/RXD0
C6	GPIO_B5/KBDIN0	G6	GPIO_A2/RXD1
C7	GPIO_B4/KBDOUT4	G7	TEST
D1	RF_XEN/GPIO_B26		
D2	IOVDD		
D3	GND		
D4	GND		
D5	GND		
D6	IOVDD		
D7	GPIO_A10/TIN1		

Table 4. uN8130-B49 Ball-Out Description

The ball-out for the B144 package option is listed in the table below. Note that "NC" implies no connection.

Ball	Name	Ball	Name
A1	XRESET	G1	D10
A2	SPI1_CLK	G2	D9
A3	SPI1_SDO	G3	D8
A4	RTC_XIN	G4	NC
A5	RF_XEN/GPIO_B24	G5	GND
A6	GPIO_B22/SPI2_XCS3	G6	GND
A7	GPIO_B20/SPI2_XCS1	G7	GND
A8	GPIO_B18/SPI2_SDI	G8	GND
A9	GPIO_B16/SPI2_CLK	G9	GND
A10	GPIO_B14/SPI1_SDO	G10	GPIO_A9/TCAP0
A11	GPIO_B13/SPI1_CLK	G11	GPIO_A10/TIN1
A12	GPIO_B11/SPI1_XCS1	G12	GPIO_A11/TCAP1
B1	QMAGN	H1	D7
B2	QSIGN	H2	D6
B3	SPI1_XCS3	H3	D5
B4	RTC_XOUT	H4	NC
B5	RF_EN/GPIO_B23	H5	NC
B6	GPIO_B21/SPI2_XCS2	H6	IOVDD
B7	GPIO_B19/SPI2_XCS0	H7	GND
B8	GPIO_B17/SPI2_SDO	H8	DVDD
B9	GPIO_B15/SPI1_SDI	H9	IOVDD
B10	GPIO_B12/SPI1_XCS2	H10	NC
B11	GPIO_B10/SPI1_XCS0	H11	GPIO_A7/PPS
B12	GPIO_B9/KBDIN4	H12	GPIO_A8/TIN0
C1	IMAGN	J1	D4
C2	ISIGN	J2	D3
C3	NC	J3	D2
C4	NC	J4	NC
C5	NC	J5	NC
C6	NC	J6	DVDD
C7	NC	J7	IOVDD
C8	NC	J8	IOVDD
C9	NC	J9	GND
C10	GPIO_B8/KBDIN3	J10	NC
C11	GPIO_B7/KBDIN2	J11	GPIO_A5/PM0
C12	GPIO_B6/KBDIN1	J12	GPIO_A6/PM1

Ball	Name	Ball	Name
D1	RF_EN/GPIO_B25	K1	D1
D2	MCLK	K2	D0
D3	NC	K3	XRD
D4	NC	K4	NC
D5	NC	K5	A12
D6	NC	K6	A9
D7	NC	K7	A6
D8	NC	K8	A1
D9	NC	K9	XCS2
D10	GPIO_B5/KBDIN0	K10	XWT
D11	GPIO_B4/KBDOUT4	K11	GPIO_A2/RXD1
D12	GPIO_B3/KBDOUT3	K12	GPIO_A4/FCLK
E1	D14	L1	XWR
E2	D15	L2	A19
E3	RF_XEN/GPIO_B26	L3	A16
E4	NC	L4	A14
E5	IOVDD	L5	A11
E6	XVDD (PLL POWER)	L6	A8
E7	NC	L7	A5
E8	IOVDD	L8	A2
E9	NC	L9	XCS3
E10	GPIO_B2/KBDOUT2	L10	XCS0
E11	GPIO_B1/KBDOUT1	L11	GPIO_A0/RXD0
E12	GPIO_B0/KBDOUT0	L12	GPIO_A3/TXD1
F1	D13	M1	A18
F2	D12	M2	A17
F3	D11	M3	A15
F4	NC	M4	A13
F5	GND	M5	A10
F6	GND	M6	A7
F7	DVDD	M7	A4
F8	IOVDD	M8	A3
F9	NC	M9	A0
F10	GPIO_A14/MMC_DATA	M10	XCS1
F11	GPIO_A13/MMC_CMD	M11	TEST
F12	GPIO_A12/MMC_CLK	M12	GPIO_A1/TXD0

Table 5. uN8130-B144 Ball-Out Description

The ball-out for the B121 package option is listed in the table below. Note that "NC" implies no connection. The ballout below does not list the alternate function.

Ball	Name	Ball	Name
A1	NC	G1	D4
A2	XVDD (PLL POWER)	G2	D6
A3	XRESET	G3	D7
A4	RTC_OUT	G4	IOVDD
A5	RTC_IN	G5	GND
A6	GPIO_B21	G6	DVDD
A7	GPIO_B17	G7	GND
A8	GPIO_B14	G8	GPIO_A7
A9	GPIO_B11	G9	GPIO_A8
A10	GPIO_B9	G10	GPIO_A6
A11	NC	G11	GPIO_A9
B1	QMAGN	H1	D5
B2	QSIGN	H2	D3
B3	SPI1_SCK	H3	D2
B4	SPI1_SDO	H4	A15
B5	GPIO_B23	H5	IOVDD
B6	GPIO_B20	H6	GND
B7	GPIO_B18	H7	GND
B8	GPIO_B15	H8	IOVDD
B9	GPIO_B12	H9	GPIO_A5
B10	GPIO_B8	H10	GPIO_A3
B11	GPIO_B7	H11	GPIO_A4
C1	MCLK	J1	D1
C2	IMAGN	J2	D0
C3	ISIGN	J3	A18
C4	SPI1_XCS3	J4	A12
C5	GPIO_B24	J5	A9
C6	GPIO_B22	J6	A6
C7	GPIO_B16	J7	A3
C8	GPIO_B13	J8	A0
C9	GPIO_B10	J9	GPIO_A0
C10	GPIO_B6	J10	GPIO_A1
C11	GPIO_B4	J11	GPIO_A2
D1	D15	K1	XRD
D2	RF_XEN	K2	XWR
D3	RF_EN	K3	A16

Ball	Name	Ball	Name
D4	GND	K4	A13
D5	GND (PLL)	K5	A10
D6	IOVDD	K6	A8
D7	GPIO_B19	K7	A4
D8	IOVDD	K8	A1
D9	GPIO_B5	K9	XCS2
D10	GPIO_B2	K10	XWT
D11	GPIO_B3	K11	TEST
E1	D12	L1	NC
E2	D13	L2	A19
E3	D11	L3	A17
E4	D14	L4	A14
E5	IOVDD	L5	A11
E6	DVDD	L6	A7
E7	GND	L7	A5
E8	GPIO_A13	L8	A2
E9	GPIO_B1	L9	XCS3
E10	GPIO_A14	L10	XCS1
E11	GPIO_B0	L11	XCS0
F1	D9		
F2	D10		
F3	D8		
F4	IOVDD		
F5	DVDD		
F6	GND		
F7	DVDD		
F8	GND		
F9	GPIO_A12		
F10	GPIO_A11		
F11	GPIO_A10		

Table 6. uN8130-B121 Ball-Out Description

Ball	Name	Ball	Name
A1	QSIGN	A8	GPIO_B19/SPI2_XCS0
B1	QMAGN	B8	GPIO_B18/SPI2_SDI
C1	GND	C8	GPIO_B20/SPI2_XCS1
D1	MCLK	M8	A6
E1	D15	N8	A7
F1	D12	P8	IOVDD
G1	IOVDD	A9	GPIO_B17/SPI2_SDO
H1	D9	B9	GPIO_B16/SPI2_CLK
J1	D7	C9	GPIO_B15/SPI1_SDI
K1	D4	M9	A3
L1	D3	N9	A4
M1	D1	P9	A5
N1	IOVDD	A10	IOVDD
P1	XRD	B10	GPIO_B14/SPI1_SDO
A2	XVDD (PLL POWER)	C10	GPIO_B12/SPI1_XCS2
B2	ISIGN	M10	A0
D2	IMAGN	N10	DVDD
E2	D14	P10	A2
F2	D13	A11	GPIO_B13/SPI1_CLK
G2	D11	B11	GPIO_B11/SPI1_XCS1
H2	D8	C11	GPIO_B10/SPI1_XCS0
J2	D6	M11	XCS2
K2	GND	N11	XCS3
L2	DVDD	P11	A1
N2	XWR	A12	GND
P2	A19	D12	GPIO_B5/KBDIN0
A3	pll_vssa	E12	GPIO_B4/KBDOUT4
D3	RF_EN/GPIO_B25	F12	GPIO_B1/KBDOUT1
E3	RF_XEN/GPIO_B26	G12	GPIO_A13/MMC_CMD
F3	No connect	H12	GPIO_A10/TIN1

G3	D10	J12	GPIO_A5/PM0
H3	No connect	K12	GPIO_A2/RXD1
J3	D5	L12	GPIO_A0/RXD0
K3	D2	P12	GND
L3	D0	A13	GPIO_B9/KBDIN4
P3	GND	B13	GPIO_B8/KBDIN3
A4	SPI1_XCS3	D13	DVDD
B4	SPI1_CLK	E13	GPIO_B3/KBDOUT3
C4	XRESET	F13	GPIO_B0/KBDOUT0
M4	A18	G13	GPIO_A11/TCAP1
N4	A17	H13	GPIO_A8/TIN0
P4	A15	J13	GPIO_A6/PM1
A5	RTC_XOUT	K13	GPIO_A4/FCLK
B5	IOVDD	L13	GPIO_A1/TXD0
C5	SPI1_SDO	N13	XCS0
M5	A16	P13	XCS1
N5	A14	A14	GPIO_B7/KBDIN2
P5	A13	B14	GPIO_B6/KBDIN1
A6	RF_XEN/GPIO_B24	C14	IOVDD
B6	DVDD	D14	GND
C6	RTC_XIN	E14	GPIO_B2/KBDOUT2
M6	A12	F14	GPIO_A14/MMC_DATA
N6	A11	G14	GPIO_A12/MMC_CLK
P6	A10	H14	GPIO_A9/TCAP0
A7	GPIO_B22/SPI2_XCS3	J14	GPIO_A7/PPS
B7	GPIO_B21/SPI2_XCS2	K14	GND
C7	RF_EN/GPIO_B23	L14	GPIO_A3/TXD1
M7	A8	M14	IOVDD
N7	A9	N14	TEST
P7	GND	P14	XWT

Table 7. uN8130-WLP Ball-Out Description

Memory Mapped Registers

The detailed functionalities of all peripheral devices are explained in detail in the uN8130 User Manual. The following table contains a summary of all memory-mapped peripheral registers in the device.

Name	Type	Bits	Description
INT_ENA0	R/W	16	Interrupt Enable Register 0
INT_ENA1	R/W	16	Interrupt Enable Register 1
INT_ENA2	R/W	16	Interrupt Enable Register 2
INT_ENA3	R/W	16	Interrupt Enable Register 3
INT_ORIG0	R/W	16	Interrupt Origin Register 0
INT_ORIG1	R/W	16	Interrupt Origin Register 1
INT_VECTOR	R	5	Interrupt source
INT_ENCOUNT	R	3	Current value of the counter
INT_DEC	W	16	Writing decrements interrupt enable counter
INT_INC	W	16	Writing increments interrupt enable counter
ICD_CTRL	R/W	8	IF signal bit counter control
ICD_IS_CNTR	R	16	I-branch sign bit count
ICM_IM_CNTR	R	16	I-branch magnitude bit count
ICD_QS_CNTR	R	16	Q-branch sign bit count
ICD_QM_CNTR	R	16	Q-branch magnitude bit count
RS0_DATA_LO	R/W	8	UART0 Data register, LSB version
RS0_DATA_HI	R/W	8	UART0 Data register, MSB version
RS0_CONF1	R	13	UART0 TX configuration/status
	R/W	12 11 10 9:0	UART0 TX-data reg full UART0 Transmitter busy UART0 Transmitter overflow UART0 Pre-divider
RS0_CONF2	R	12	UART0 RX configuration/status
	R/W	11 10 9 8 7:0	UART0 RX-data is valid UART0 is receiving data UART0 RX overflow error UART0 Stop-bit of the frame UART0 Freq divider value
RS1_DATA_LO	R/W	8	UART1 Data register, LSB version
RS1_DATA_HI	R/W	8	UART1 Data register, MSB version
RS1_CONF1	R	13	UART1 TX configuration/status
	R/W	12 11 10 9:0	UART1 TX-data reg full UART1 Transmitter busy UART1 Transmitter overflow UART1 Pre-divider
RS1_CONF2	R	13	UART1 RX configuration/status

Name	Type	Bits	Description
	R/W	12 11 10 9 8 7:0	UART1 Generate FCLK UART1 RX-data is valid UART0 is receiving data UART1 RX overflow error UART1 Stop-bit of the frame UART1 Freq divider value
PM0_CONF	R/W	6	PM0 configuration register
	R	5 4 3:2 1:0	Current input (after inversion), read-only Invert input Trigger mode Accuracy mode
PM0_HIGH	R/W	15:0	How many cycles input was high
PM0_LOW	R/W	15:0	How many cycles input was low
PM0_CNT	R	15:0	Current value of counter
PM1_CONF	R/W	6	PM1 configuration register
	R	5 4 3:2 1:0	Current input (after inversion), read-only Invert input Trigger mode Accuracy mode
PM1_HIGH	R/W	15:0	How many cycles input was high
PM1_LOW	R/W	15:0	How many cycles input was low
PM1_CNT	R	15:0	Current value of counter
TIMER_ENA	R/W	4	Timer enable register
TME0	R/W	16	Clock cycle counter
TME1	R/W	16	Epoch counter
TMED_DELAY	R/W	16	Delay configuration
TME2	R/W	16	Epoch counter reload value, 32735 after reset
TMG0_CTRL	R/W	7	TMG0 control register
TMG0_INT_ORIG	R/W	2	TMG0 interrupt origin register
TMG0_CAPTURE	R	16	TMG0 capture register
TMG0_SCALE	R/W	8	TMG0 prescaler
TMG0_INIT	R/W	16	TMG0 initial value
TMG0_DELAY	R/W	16	TMG0 delay configuration
TMG1_CTRL	R/W	7	TMG1 control register
TMG1_INT_ORIG	R/W	2	TMG1 interrupt origin register
TMG1_CAPTURE	R	16	TMG1 capture register
TMG1_SCALE	R/W	8	TMG1 prescaler
TMG1_INIT	R/W	16	TMG1 initial value
TMG1_DELAY	R/W	15	TMG1 delay configuration
GPIOA_BIT_CTRL0	R/W	10	Bit control for bit 0
GPIOA_BIT_CTRL1	R/W	10	Bit control for bit 1
GPIOA_BIT_CTRL14	R/W	10	Bit control for bit 14
GPIOA_DATA_IN0	R	15	Data in, bits 14-0
GPIOA_INT_ORIG0	R/W	15	Interrupt origin, bits 14-0

Name	Type	Bits	Description
GPIOA_DIR0	R/W	15	Direction control, bits 14-0
GPIOA_DEVSEL0	R/W	15	Selection control, bits 14-0
GPIOA_DATA_OUT0	R/W	15	Data out, bits 14-0
MMC_CLK_REG	R/W	10	Clock divider register
MMC_INT_CTRL	R/W	4	Interrupt control register
MMC_DRV_STAT	R	7	Driver status register
MMC_DAT_CTRL	R	14	DAT-line control register
MMC_CALC_CRC	R	16	Calculated CRC for data block
MMC_RCV_CRC	R	16	Received CRC for data block
MMC_DAT_CNT	R	7	Data byte and bit counters
MMC_DAT_BL	W	12	Data block size
MMC_CMD_CTRL	R	16	CMD-line control register
MMC_RSP0	R/W	16	Cmd/response register 0
MMC_RSP1	R/W	16	Cmd/response register 1
MMC_RSP2	R/W	16	Cmd/response register 2
MMC_RSP3	R	16	Response register 3
MMC_DATA0	R/W	16	Data register 0, bits 15:0
MMC_DATA1	R/W	16	Data register 1, bits 31-16
MMC_DATA2	R/W	16	Data register 2, bits 47-32
MMC_DATA3	R/W	16	Data register 3, bits 63-48
PPS_CONF	R/W	16	PPS signal generator configuration
PPS_LENGTH	R/W	16	Pulse length in clock cycles
PPS_CNT	R	16	Current PPS counter value
PPS_STATUS	R	3	PPS status register
BCR0	R/W	16	Bus control register 0
BCR1	R/W	1	Bus control register 1
GPIOB_BIT_CTRL0	R/W	10	Bit control for bit 0
GPIOB_BIT_CTRL26	R/W	10	Bit control for bit 26
GPIOB_DATA_IN0	R	16	Data in, bits 15-0
GPIOB_DATA_IN1	R	10	Data in, bits 26-16
GPIOB_INT_ORIG0	R/W	16	Interrupt origin, bits 15-0
GPIOB_INT_ORIG1	R/W	10	Interrupt origin, bits 26-16
GPIOB_DIR0	R/W	16	Direction control, bits 15-0
GPIOB_DIR1	R/W	10	Direction control, bits 26-16
GPIOB_DEVSEL0	R/W	16	Selection control, bits 15-0
GPIOB_DEVSEL1	R/W	10	Selection control, bits 26-16
GPIOB_DATA_OUT0	R/W	16	Data out, bits 15-0
GPIOB_DATA_OUT1	R/W	10	Data out, bits 26-16
SPI1_CONF	W	15	SPI1 configuration
SPI1_STATUS	R/W	13	SPI1 status register
SPI1_DIV	W	10	SPI1 divider configuration
SPI1_DATA	R/W	16	SPI1 data register

Name	Type	Bits	Description
SPI2_CONF	W	15	SPI2 configuration
SPI2_STATUS	R/W	13	SPI2 status register
SPI2_DIV	W	11	SPI2 divider configuration
SPI2_DATA	R/W	16	SPI2 data register
MIXER_FREQ	R/W	16	Input mixer frequency shift configuration
KEYBOARD	R/W	8	Keycode of the key pressed
SLEEP_DATA	R/W	16	SLP1 Sleep timer data register
SLEEP_CONT	R/W	4	SLP1 Counter control/status
SLEEP_CNT	R	16	SLP1 Current timer value
SLEEP_DATA	R/W	16	SLP2 Sleep timer data register
SLEEP_CONT	R/W	4	SLP2 Counter control/status
SLEEP_CNT	R	16	SLP2 Current timer value
SLEEP_DATA	R/W	16	SLP3 Sleep timer data register
SLEEP_CONT	R/W	4	SLP3 Counter control/status
SLEEP_CNT	R	16	SLP3 Current timer value
SLEEP_DATA	R/W	16	SLP4 Sleep timer data register
SLEEP_CONT	R/W	4	SLP4 Counter control/status
SLEEP_CNT	R	16	SLP4 Current timer value
RTC_DATA_HI	R/W	16	RTC counter register
RTC_DATA_LO	R/W	15	RTC counter register (n/32768 of second)
RTC_ALARM_HI	R/W	16	RTC alarm register
RTC_ALARM_LO	R/W	15	RTC alarm register (n/32768 of second)
RTC_STATUS	R/W	5	RTC status register
		4:3	Current state of alarm update 00 = normal 01 = prewrite 10 = write high buffer 11 = write low buffer
		2:0	Current state of RTC counter 000 = normal 001 = prewrite 010 = write high buffer 011 = write low buffer 100 = updating RTC counter
SYS_CTRL	R/W	14	System control register
PERIPH_ENA	R/W	14	Peripheral device clock enable bits
SLEEP_DELAY	R/W	15	Sleep mode wakeup delay
SYS_CFG	R/W	3	Misc. config bits
WD_INTERV	R/W	16	Watchdog interval configuration
WD_CMD	W	16	Watchdog command register
WD_CNT	R	16	Watchdog Current counter value
SE_CONF	R/W	16	SE configuration
SE_CFREQ_LO	W	8	SE code frequency, low part

Name	Type	Bits	Description
SE_CFREQ_HI	W	16	SE code frequency, high part
SE_FREQ	W	16	SE coarse carrier replica frequency
SE_SEQ	W	10	SE G2 PRN generator initial state
SE_COH	W	7	SE coherent integration length
SE_NONCOH	W	9	SE non-coherent integration length
SE_MFP0_FREQ	W	16	SE fine carrier replica frequency
SE_MFP1_FREQ	W	16	SE fine carrier replica frequency
SE_MFP2_FREQ	W	16	SE fine carrier replica frequency
SE_MFP3_FREQ	W	16	SE fine carrier replica frequency
SE_MAX_PHASE0	R	11	SE position of maximum integration result
SE_ACQ_MAX0	R	16	SE value of maximum integration result
SE_SUM_LO0	R	16	SE sum of results, low part
SE_SUM_HI0	R	16	SE sum of results, high part
SE_SAT_CNT0	R	10	SE result saturation count
SE_MAX_PHASE1	R	11	SE position of maximum integration result
SE_ACQ_MAX1	R	16	SE value of maximum integration result
SE_SUM_LO1	R	16	SE sum of results, low part
SE_SUM_HI1	R	16	SE sum of results, high part
SE_SAT_CNT1	R	10	SE result saturation count
SE_MAX_PHASE2	R	11	SE position of maximum integration result
SE_ACQ_MAX2	R	1	SE value of maximum integration result
SE_SUM_LO2	R	16	SE sum of results, low part
SE_SUM_HI2	R	16	SE sum of results, high part
SE_SAT_CNT2	R	10	SE result saturation count
SE_MAX_PHASE3	R	11	SE position of maximum integration result
SE_ACQ_MAX3	R	16	SE value of maximum integration result
SE_SUM_LO3	R	16	SE sum of results, low part
SE_SUM_HI3	R	16	SE sum of results, high part
SE_SAT_CNT3	R	10	SE result saturation count
CH_ENABLE	R/W	12	Channel enable bits
CORR_INT_ORIG	R/W	12	Correlator interrupt origin

Table 8. Memory Mapped Registers

The correlator unit has a separate set of registers for each channel. The set of registers for each correlator is listed in the following table.

Name	Type	Bits	Description
CH_LO_FREQ_LO	W	8	Carrier replica frequency, low
CH_LO_FREQ_HI	W	16	Carrier replica frequency, high
CH_PRN_FREQ_LO	W	12	PRN frequency, low
CH_PRN_FREQ_HI	W	16	PRN frequency, high
CH_PRN_SEQ	W	10	PRN generator initial value
CH_PRN_IPHASE	W	8	PRN NCO phase initialization values
CH_SETTER_IPHASE	W	11	Setter phase initialization values
CH_LO_IPHASE	W	8	Carrier accumulator initial value
CH_CORR_CONF	W	16	PRN code masking configuration
CH_CONF	W	2	Shift register clocking speed
CH_IE2_DATA	R	16	I-branch correlation result early 2
CH_QE2_DATA	R	16	Q-branch correlation result early 2
CH_IE1_DATA	R	16	I-branch correlation result early 1
CH_QE1_DATA	R	16	Q-branch correlation result early 1
CH_IL1_DATA	R	16	I-branch correlation result late 1
CH_QL1_DATA	R	16	Q-branch correlation result late 1
CH_IL2_DATA	R	16	I-branch correlation result late 2
CH_QL2_DATA	R	16	Q-branch correlation result late 2
CH_LO_PHASE	R	16	Carrier replica accumulator, low
CH_LO_COUNT	R	16	Carrier replica accumulator, high
CH_PRN_PHASE	R	16	PRN phase, 16 MSBs
CH_PRN_CHIP	R	16	PRN data sampling time (chip number)
CH_PRN_COUNT	R	16	Code cycle count

Table 9. Correlator Register Set for Each Channel

Interconnection with u-Nav RFIC

The u-Nav uN802x and uN100x family of GPS RF front-end chips such as the uN8021C can be connected to the *uN8130* GPS baseband processor using nine digital signals as shown in the figure below. No external glue logic is required; however, see u-Nav application notes discussing RF path design and recommendations for noise reduction. The digital signals can be divided into three separate functional groups as follows:

- System signals (clock and RF enable)
- Data signals from RF to baseband (I/Q sign and magnitude)
- Control signals from baseband to RF (SPI interface)

The block diagram below shows this interconnection with an uN8021. The interface is the same with an uN100x.

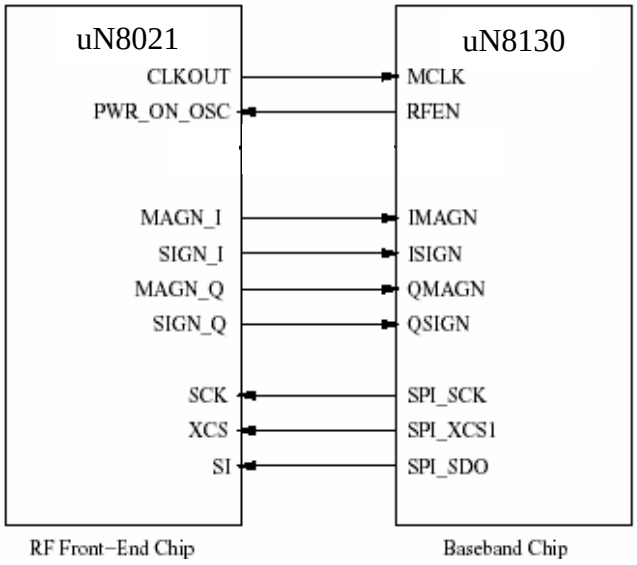


Figure 7. Interconnection Diagram with uN802x

There are many options in implementing the SPI interface signals to the RFIC. The following clarifies these options with the recommendations:

- 144 Package – use dedicated SPI1_CLK, SPI1_SDO, and SPI1_XCS3; RF_EN (GPIO_B23) and RF_XEN (GPIO_B24) for RFIC enable and power control.
- 49 Package – reconfigure GPIO alternate functions GPIO_B13 for SPI1_CLK, GPIO_B14 for SPIO1_SDO, and typically GPIO_B11 for SPI_XCS1. RF_EN (GPIO_B25) for RFEN and RF_XEN (GPIO_B26) for RFIC enable and power control.

On reset, GPIO_B23/ B24, B25/B26 are forced into RF_EN/RF_XEN respectively. In this device, there is no electrical difference between B23/B24 pair and B25/B26. The choice of which to use is arbitrary, though B23 and B24 are only available in 144 package.

General Description

The *uN8130* GPS Baseband Receiver implements all hardware necessary for acquiring and tracking GPS satellite signals as well as enough processing capability and memory for on-chip navigation solution computation. The uN8130 is u-Nav's 2nd generation baseband offering many features beyond those of the earlier uN8031. For programming details, refer to "uN8130 User Manual".

The *uN8130* GPS Baseband Receiver has two main functional units for GPS signal processing: dedicated search engine for satellite acquisition based on QwikLock™ technology and an array of twelve independent tracking correlators employing u-Nav Zoom Correlators™ technology. These units are controlled by a proprietary low-power DSP processor core referred as the VS_DSP. The chip has integrated program and data memories for the software and data, and interfaces to the application system via two asynchronous serial ports. There is an external memory bus for connecting non-volatile FLASH memory which will hold the DSP software and any necessary non-volatile storage requiring data. There is also a 42-pin general purpose I/O interface which enables interfacing the uN8130 to many other devices. I/O voltage including the external data bus and all GPIO pins can be operated at either 1.8V or 3V; however, mixed I/O levels of 1.8V and 3V is not supported. The 1PPS output is capable of delivering an accurate time mark signal if required by the application. Multi Media Card (MMC) interface is included for removable storage applications. Extensive user timers and a watchdog timer provide extensive control capability. The device includes an operating mode enabling interface to low cost IrDA transceivers. Direct keyboard interface up to a 5x5 array is supported. The *uN8130* has extensive and flexible power control which enables extremely low-power GPS receiver operation. This is required by many portable applications where power is at premium. Even with low-power operation, the *uN8130* still features high performance.

Internal Memory

The uN8130 contains the following internal static memories:

- 8k x 32b program RAM memory (I-RAM)
- 4k x 32b program RAM memory (I-RAM)
- 8k x 32b program ROM memory (I-ROM)
- 32k x 16b X-data RAM memory (X-RAM)
- 16k x 16b Y-data RAM memory (Y-RAM)
- 8k x 16b Y-data ROM memory (Y-ROM)
- 8k x 32b RAM search memory (S-MEM)

In the VS_DSP architecture, all peripheral devices have a memory-mapped register interface and possibly memory areas shared with the processor. Thus, in addition to actual memories there are two I/O device register areas in the memory map of the uN8130. The I/O memory in the Y-memory is used for accessing internal peripheral devices, while the Ext I/O area is for external peripherals connected to the external bus.

The memory map of uN8130 is shown in figure 8. The 8k and 4k I-RAMs are mirrored in the X- and Y-memory. 16 MSBs of each 32-bit instruction word are mirrored in the X-memory and 16 LSBs in the Y-memory. I-memory address 0x0000 is mirrored in X- and Y-memory address 0x8000, 0x0001 in 0x8001 and so forth.

The first 1kW of the I-ROM can be made visible in the addresses 0x0000-0x0fff by setting *ena_rom* bit of the system control register SYS_CTRL to one. This is the default value at reset, and the first 1kW of I-ROM can thus be used a boot-ROM. Setting *ena_rom* to zero makes the first kW of RAM visible. Note that the whole of the 8kW I-ROM is always visible in the addresses 0x6000-0x7fff.

The internal I-RAM space can be reconfigured to be 12KW or 16KW depending on the setting of the *Swap* bit in SYS_CTRL register. On reset, Swap = 0 thereby resulting in the 12KW memory map shown in figure 8. When programmed with Swap = 1, then the I-RAM space becomes 16KW at the expense of a 4KW reduction to both the X and Y memory spaces.

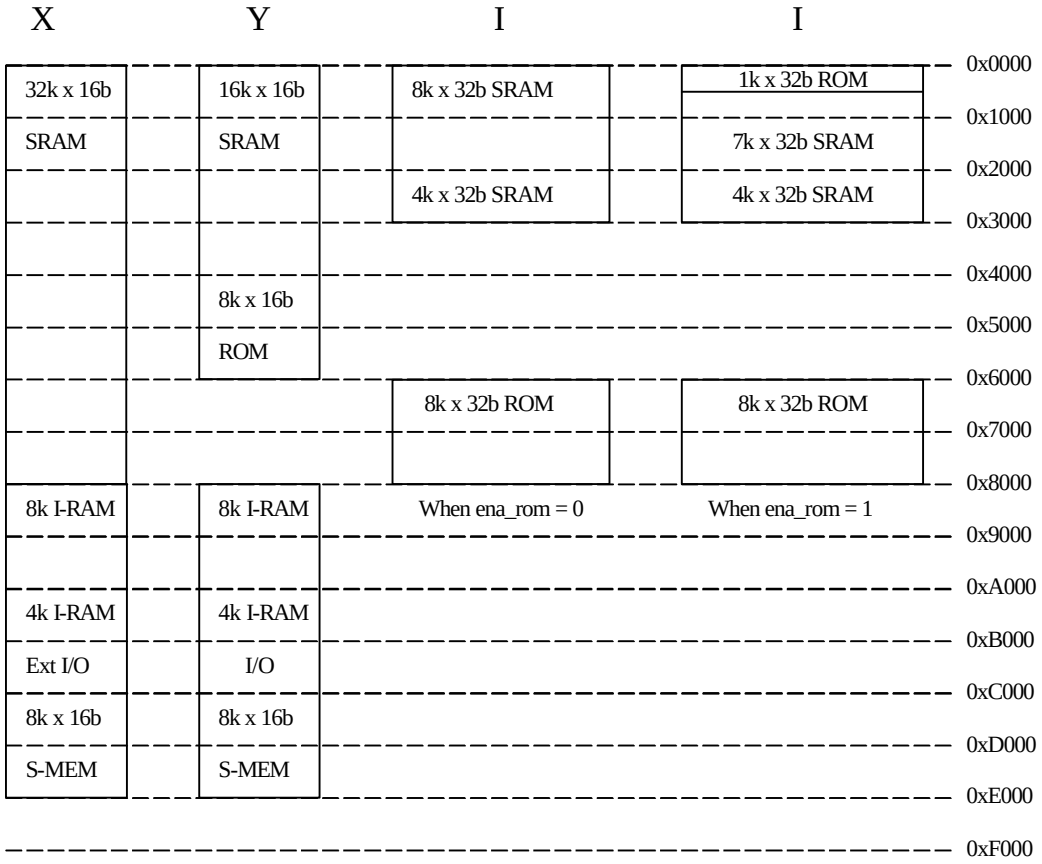


Figure 8. Memory map of the uN8130 (Swap = 0)

VS_DSP Core

The uN8130 includes a VS_DSP processor for receiver control, peripheral control, data communications and navigation solution calculation. This embedded processor architecture is illustrated in figure 9.

The VS_DSP clock rate is 2 x MCLK yielding a clock frequency approximately 32MHz. This 2 x clock is generated from an on-chip PLL, doubling MCLK input. It features a three-stage pipeline performing fetch, decode, and execution simultaneously. In single clock cycle, the VSP_DSP can do the following:

Generate next address
Fetch a new instruction
Decode previous instruction
Perform two data moves
Post-modify two pointers
Perform register computation

The processor architecture implements two 16-bit wide data buses X and Y. Two dedicated address calculation units enable two operands fetched in parallel. The instruction set features seven addressing modes and eight index registers. Each

instruction is a 32 bit program word and is fetched as a 32-bit word from internal memory but is broken into two successive 16-bit fetches from external memory. The multiplier performs 16 bit signed or unsigned, integer or fractional, saturating or unsaturated multiplication with 32 bit result. The ALU performs signed arithmetic, logical operations, manipulation of status flags and mode bits, and multiple-and-accumulation MAC with saturation. There are eight guard bits in each of the eight arithmetic registers. The VS_DSP core features barrel shifter, bit-reverse addressing modes, and zero overhead loop control. External data and instruction memory access enables large flash memory based program development including wait state generation. C language development tool support for Unix and PC platforms.

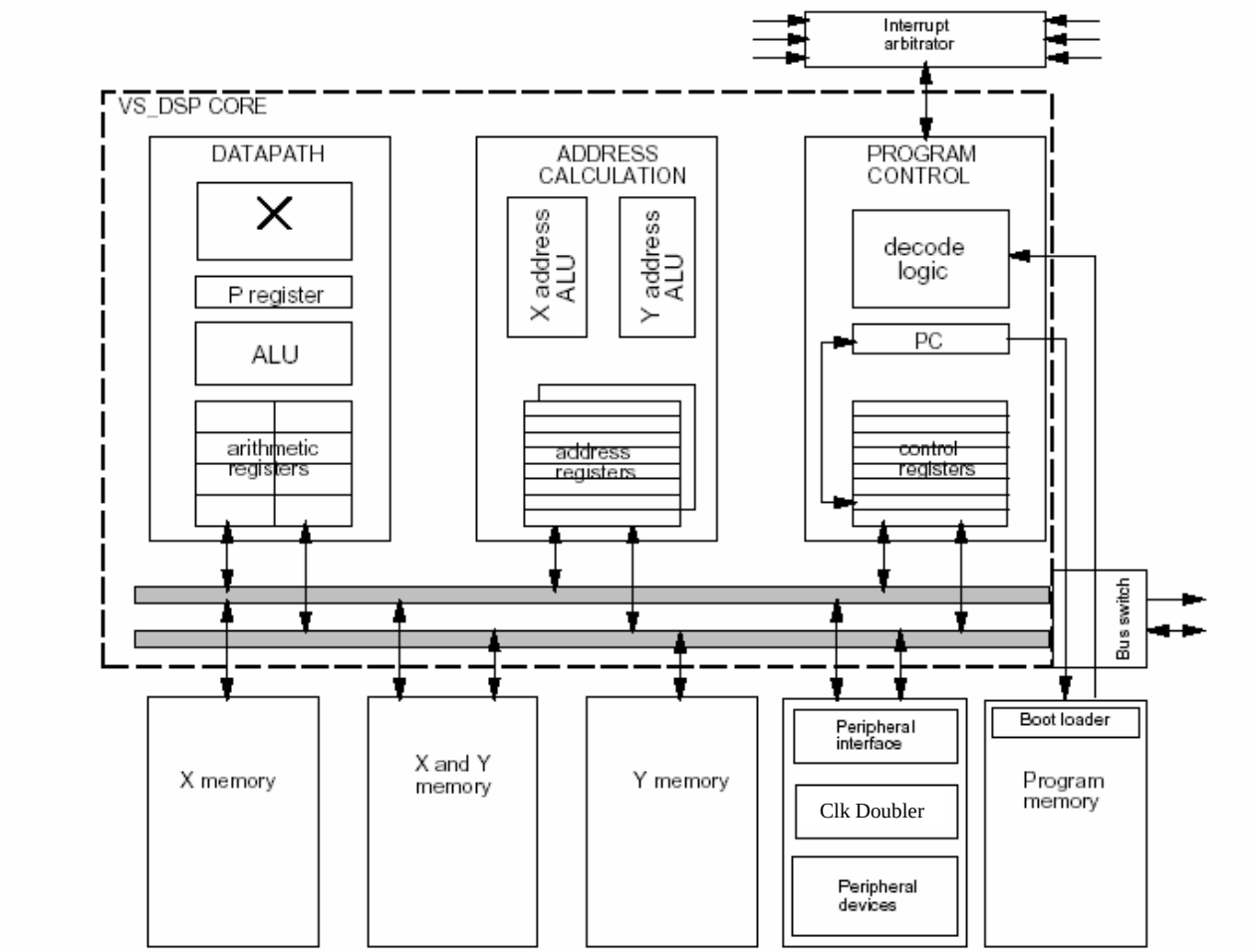


Figure 9. General VS_DSP Architecture

Search Engine

The Search Engine is the u-Nav Microelectronics developed rapid acquisition block. The search engine implements acquisition frequency analysis and signal integration. The baseband receives two quadrature 2-bit I/Q inputs from the RF chip. Programmable doppler frequency determines the frequency bin searched. The Search Engine performs

code-phase analysis at ½ chip resolution for all 1023 code phases yielding 2046 sample outcomes. The uN8130 features four integration channels for simultaneous searching of up to four frequency bins. Pre-detection coherent integration time can be configured to be 1 to128 ms. Post-detection non-coherent integration in configurable as 1 to 512 rounds. The Search Engine results are written to dedicated on-chip memory (S-MEM). S-MEM is accessible by the VS_DSP for search algorithm implementation. The integration periods be synchronized to known bit timing and is autonomous in operation, generating an interrupt upon completion.

There is a set of six registers for each of the four integration channels, one configuration register and five result registers. Additionally, there are seven configuration registers that affect the whole search engine. The correlation channels are numbered 0-3, and so are the registers that correspond to them.

Correlator Unit

The correlator unit implements the hardware for baseband tracking via twelve parallel hardware correlation channels using Zoom Correlators™. The main features of the correlator unit are:

- 2-bit I/Q inputs
- 12 parallel tracking channels
- Four Zoom Correlators(TM) per tracking channel
- Individual channels can be enabled or disabled for saving power
- Easy setting of tracking state for rapid signal acquisition

Mixed individual and common dump: all channel output data is sampled synchronized to that channel's code generator epoch timing, one interrupt is generated with an interrupt source register indicating the channel which generated the interrupt. All measurement data (code and carrier counts and phases) are sampled simultaneously for all channels. Only one interrupt is generated. The dump rate is configurable.

Input Mixer

The Input Mixer block is essentially a digital mixer and is located in front of ICD, Search Engine and Correlator. It is intended for common mode IF frequency offset control.

System Controller

The uN8130 powerdown and operation mode is handled by the system controller. Unmentioned bits the system control registers are reserved and should always be set to zero.

The uN8130 can reduce power consumption by disabling individual peripheral devices and halting the CPU. In the halt-state the CPU and memories are not clocked, but the peripherals are clocked and can wake up CPU by generating an interrupt. Some of peripheral devices can be disabled and enabled using the peripheral enable register. Timers have their own enable register. The rest of the peripherals go into power-down

mode when they are idle, and are automatically activated when peripherals' configuration registers are written or activated by other peripherals.
When waking from sleep mode, the RF enable signal RF_EN and its inverse RF_XEN can be activated before the baseband chip itself will awaken. This gives time to clock generation start up and stabilize before the baseband chip is activated. The delay between RF_EN/RF_XEN activation and the baseband chip activation (processor and peripherals) can be specified using the sleep mode wakeup delay register. The delay counter is clocked by the RTC unit, and the delay unit is therefore the same as the RTC unit clock cycle, i.e. 1/32768th of a second. The delay is adjustable to four different intervals.

PPS

The PPS unit is used for generating a timing pulse, typically once per second. The unit supports both sub-millisecond and multi-millisecond pulse lengths, and the pulse frequency is completely software controlled. The pulse start and end can be timed with MCLK clock cycle accuracy, referenced to the epoch pulse generated by the TME clock unit.

SPI 1

The SPI 1 unit implements a general-purpose SPI master serial interface supporting four slave devices. Only one of the devices can be accessed at a time. The interface has the following signal lines:

Name	Description
SPI1_SCK	Clock output
SPI1_XCS0	Chip select 0 (EEPROM)
SPI1_XCS1	Chip select 1 (Other)
SPI1_XCS2	Chip select 2 (Other)
SPI1_XCS3	Chip select 3 (External RF)
SPI1_SDI	Data input
SPI1_SDO	Data output

Table 10. SPI 1 Signal Lines

The SPI1_SDI pin should be programmed as input with pull-up resistor. Since the internal pull-up is 100K ohms, it may be necessary to add an external pull-up for speeds greater than 500KHz.

SPI 2

The SPI 2 unit implements a general-purpose SPI master serial interface supporting interfacing with four slave devices or one master device. The interface has following signal lines:

Name	Description
SPI2_SCK	Clock input/output
SPI2_XCS0	Chip select output
SPI2_XCS1	Chip select output
SPI2_XCS2	Chip select output
SPI2_XCS3	Chip select output or input (slave mode)
SPI2_SDI	Data input
SPI2_SDO	Data output

Table 11. SPI 2 Signal Lines

The SPI2 interface mode is programmable only as a master. The SPI2 will drive the clock and chip select lines. SPI2 operates exactly like SPI1.

The SPI2_SDI pin should be programmed as input with pull-up resistor. Since the internal pull-up is nominally 74K ohms, it may be necessary to add an external pull-up for speeds greater than 500KHz.

MMC

The MMC unit implements a standard 3-wire MultiMediaCard serial bus interface, and provides control and data register for easy usage of the bus. Both block and stream mode data transfer is supported. The CRC is calculated automatically for transmitted commands and data blocks, also received responses and data blocks are checked for correct CRC. The MMC unit has a 64-bit data buffer and is capable of stopping bus clock to prevent buffer overflow and underflow situations.

Pin	Type	Description
MMC_CLK	O	MMC clock signal
MMC_CMD	I/O	MMC command, push-pull or open-drain operation
MMC_DAT	I/O	MMC data

Table 12. MMC Signal Lines

The MMC command signal, when used as an output, operates in push-pull during normal operation and in open-drain during bus initialization procedure. MMC clock and data lines operate always in push-pull mode when used as outputs. Note that CLK is always driven by the host and is therefore always an output. Multiple block transfer is not supported, use only single block transfer mode.

Pulse Measurement

The uN8130 has two pulse measurement devices which can be used to measure with great accuracy, how long an input stays logically high or low. Note that in the description below, the rising/falling edge is used in logical sense. If the input inversion is enabled then falling edge on input is logical rising edge.

When a pulse measurement device is enabled, it starts to wait for the first rising edge (first complete cycle to measure). When one is found a counter is started. When falling edge is detected then value of the measurement counter is captured and a new count is started. At next rising edge value of measurement counter is captured to a second register. this gives: *cycle length* = first + second count value. Each measurement unit can be configured in various modes. If the trigger mode was once-only then counter is disabled after the second capture. The counter is saturating, but different accuracy modes can be used to avoid saturation. The counter can be disabled and other counters can be used to measure time delay between interrupts if the internal counter is not suitable.

Keyboard I/O port

The keyboard controller is supports up to a 5 x 5 keyboard matrix. The controller scans the matrix and generates an interrupt when a key is pressed or released. There is a bounce-removal logic with 28 ms delay time. The controller does not support cases where multiple keys are pressed simultaneously.

The code of the key pressed can be read from a keyboard register. If a key was released, the keyboard register holds the value zero.

The keyboard controller has also combinatorial mode where all of the row select outputs are active and an interrupt is generated when any of the keys in the keyboard matrix is pressed. The combinatorial mode can also be used to wake the uN8130 from SLEEP state.

The keyboard interface output pins can be configured to be push-pull or open-drain type in the GPIO_B configuration registers. If the application doesn't use all 5 keyboard inputs, then unused pins should be configured to be used by the GPIO_B and they will be internally pulled low.

Real Time Clock

Real time clock (RTC) increments 32768 times in a second a 31-bit up counter. It has a 31-bit alarm register which can be used to generate RTC alarms. The RTC is directly clocked with the 32768 Hz RTC clock, so its resolution is 1/32768 s, giving 30.5 µs accuracy for alarms. The resolution of RTC is 1/32768 s.

UART

Two Universal Asynchronous Receiver Transmitters (UART) are available for application use. UART0 may be involved in program boot-up as determined by the uN8130 boot protocol fixed in on-chip program ROM. See uN8130 User Manual for more details regarding booting.

UART1 can be configured to generate continuous FCLK output of programmable frequency. This facilitates asynchronous IrDA interfacing to 115.2kbps with low cost external transceivers. The UARTs automatically power down when idle.

ICD

The IF signal bit counter device (ICD) counts ones in sign and magnitude bits of incoming I and Q signal in a given time interval. The values are used in configuring the gain parameters in the RF front end for Automatic Gain Control (AGC) purposes. After the given time interval has elapsed, the block generates an interrupt and four values are readable through the memory mapped register interface.

GPIO

The uN8130 has 42 general-purpose I/O pins, which are handled by two devices, GPIO_A (15 pins) and GPIO_B (27 pins). Each device has own configuration registers and interrupt signal.

The general-purpose parallel I/O ports are input/output interfaces, each bit of which can be configured as an input or output. The GPIOs can be used to connect different kind of peripherals; for example, an LCD-display to the uN8130. If a bit is configured as input, it can be configured to generate an interrupt as well. Interrupt can be configured to happen on rising, falling or on both edges of input signal.

The GPIO pins are shared with various interface peripherals. Thus, if a peripheral device is not used by an application, its I/O pins can be used as GPIO.

Timers

uN8130 contains nine separate timers, namely the epoch timer (TME), the delayed epoch timer (TMED), two general-purpose timers (TMG0 and TMG1), four sleep timers and RF wakeup signal delay timer .

The timers have their own enable register. Each control bit in the enable register starts or stops the clocks of the corresponding timer thus enabling or disabling it.

TME

It generates one epoch pulse every Nth clock cycle (N=32735 after reset, which is close to millisecond with an 16.3676 MHz input MCLK). The epoch pulse is used by the VS_DSP, search engine, correlator, ICD and 1PPS for synchronization. TME also has a 16-bit counter which counts the number of epoch pulses.

TMED

The delayed epoch timer TMED generates an interrupt after the TME-generated epoch interrupt. The delay between INT_TME and INT_TMED is configurable.

TMG0 and TMG1

The general-purpose timers (TMG0 and TMG1) have configurable prescalers and clock cycle counts. The clock input is selectable between three sources and there is a capture mode to count external events. Each timer also has a programmable delay, referenced to the epoch pulse. This makes it possible to have a specified delay between interrupts generated by the TME, TMG0, and TMG1.

Sleep timers
Sleep timers are 16-bit down counters which have a selectable resolution 7.8 ms (128 Hz) or 30.5us (32768 Hz). They generate an interrupt when they reach zero. They can also be used to wake the uN8130 from the SLEEP state.

There is a separate wake-up signal delay timer. This timer controls the sequencing associated with RF_EN/RF_XEN pins and enabling the uN8130 master clock input from MCLK.

Watchdog
uN8130 contains a watchdog peripheral, which resets the chip if not refreshed frequently enough. Basically the watchdog is a 16-bit counter with enabling, disabling and restarting controls.. The watchdog can be kept from resetting the chip by restarting is frequently enough (more often than the configured interval). The watchdog counter is clocked with the frequency of 128 Hz.

Interrupt controller
The interrupt controller is used to deliver the interrupt requests from the peripherals to the processor. Each interrupt source has own interrupt vector (start address). There are three levels of priority and a disable available for all the sources. Disabled interrupt sources can set a bit in origin registers applicable for polling.

I/Q Data Input
The intermediate frequency (IF) input from the RF front-end chip is input to the uN8130 as a pair of two-bit, quadrature digital signals. It is interpreted as a complex number consisting of real and imaginary parts, corresponding to the In-phase and Quadrature arms of the signal. The IF nominal frequency is around 38.5 kHz (for MCLK of 16.3676 MHz and driven by uN8021 RF chip). The two bits of each IF input arm are in sign-magnitude format and the bits are decoded as specified in the table below:

sign	mag	value
1	1	-3
1	0	-1
0	0	+1
0	1	+3

Table 13: I/Q Bit Decoding

External Bus Interface
External bus interface multiplexes core data buses XDB, YDB and IDB to the external (off-chip) data bus EDB. 32-bit IDB accesses are converted to 16-bit EDB accesses. In order to interface flexibly with external memories having different speeds, EDB has configurable wait states.

External bus has four programmable chip select outputs for external memory blocks. All four chip select outputs can have different amounts of wait states. In addition to this, wait states can be requested asynchronously using the XWT input pin. Chip select outputs XCS(3:0) are active low.

Addresses

Logical addresses are converted to physical addresses by the external bus interface to map all three address spaces (X,Y and I) to a single address space (E).

For external X addresses, the physical address is the logical address. For external Y addresses, the physical address is obtained by inverting logical address bit 15. Note that I-MEM and S-MEM gaps in X memory space can be hidden by setting bit 10 of SYS_CTRL register. For external I addresses, the physical address is obtained as follows:

1. The logical address is inverted.
2. The inverted address is shifted left by 1 bit.
3. The LSB is set to 0 for low 16 bit access or to 1 for high 16 bit access.

This maps the zero-page (first 64K) instruction addresses to end of external memory.

The above scheme allows both data and instruction to reside in same physical memory. Data is in the start of the memory and instructions in the end of the memory. The mapping is conceptually depicted in figure 10. This shows how I:0x0000 would be mapped to external E:0xffff ffff and E:0xffff fffe, I:0x0001 to E:0xffff fffd and E:0xffff fffc and so on. External Y-memory range Y:0x8000 to Y:0xffff is mapped to E:0x0000 to E:0x7fff. Because of internal on-chip instruction memory, the external memory from I:0x00000 through I:0x02FFF is not actually accessible as instruction memory as suggested in the figure below. Instead, this space is accessible only as X memory. Refer to the uN8130 User Manual for more detailed information regarding addressing.

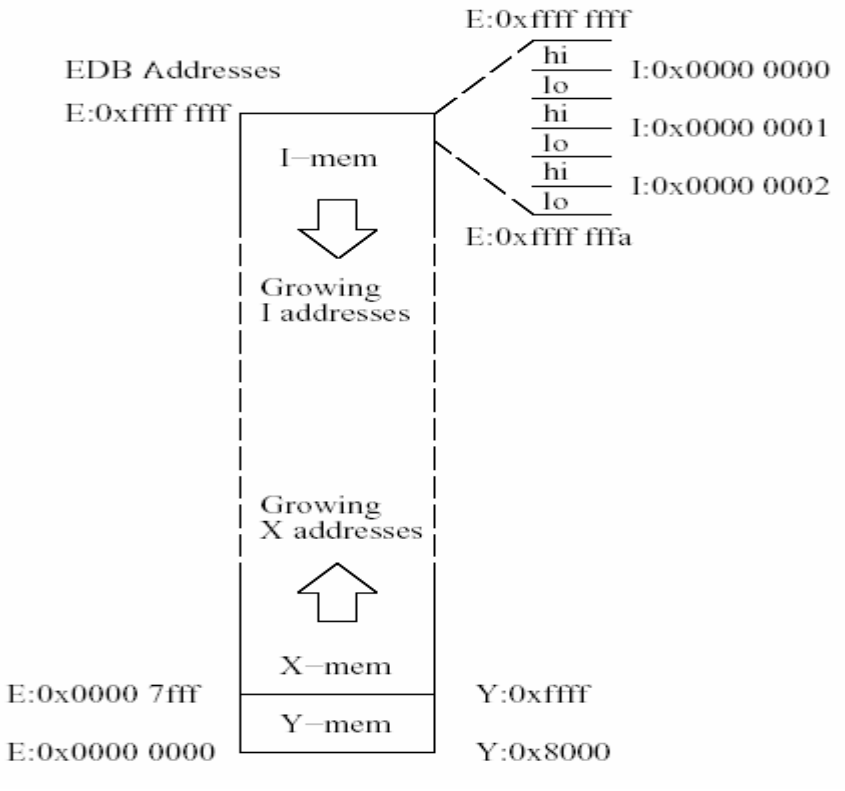


Figure 10. Internal to External Memory Space Mapping

External Data Bus Configuration Registers

The external bus interface control register is used to configure the wait states. Each chip select output XCS[3..0] has four programmable bits which contain the number of wait states to be generated for that chip select output. Each wait state corresponds to one clock cycle. At reset, the default is 15 wait states for all external memory accesses. Figure 11 illustrates a write operation with wait states. In read operations the read signal XRD has similar timing as XWR. Clocks are not part of the interface but they are included here to show how EDB access is synchronized to core clocks for conceptual understanding only.

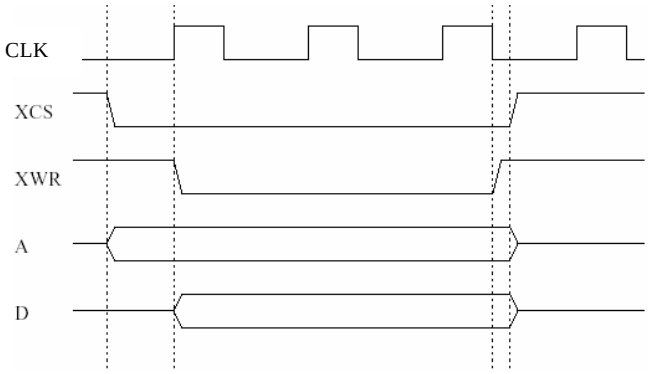


Figure 11. External Data Bus With Wait States

The chip select register is used to configure the behavior of the four chip select outputs. External memory is divided into four blocks of one mega-word each. In memory accesses, bits 21 and 20 code the chip select and bits 19-0 contain the 20-bit address shown on the external bus. The address ranges thus generated are shown in table 14 below.

Block	address range
BL0	X:0x0000 0000… 0x000F FFFF I:0x0018 0000 … 0x001F FFFF
BL1	X:0x0010 0000 … 0x001F FFFF I:0x0010 0000 … 0x0017 FFFF
BL2	X:0x0020 0000 … 0x002F FFFF I:0x0008 0000 … 0x000F FFFF
BL3	X:0x0030 0000 … 0x003F FFFF I:0x0000 0000 … 0x0007 FFFF

Table 14. External Memory blocks

It is possible to configure BL3 to be included in XCS0. This can be used if a single memory chip is used for both data and program memory.

Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	-55	+150	°C
Operating temperature	T_A	-40	+85	°C
Peak Reflow Temperature, < 10 sec	$T_{PEAK-BGA}$ $T_{PEAK-WLP}$		222 260	°C
Power Dissipation (Ta = +85 °C)	P_D		500	mW
Current on any pin to avoid latch-up (Latch up compliance: JESD-78 Class I)	I_{MAX}	-100	+100	mA
ESD protection	V_{ESD}	1000		V
Supply Voltage, digital core	DVDD	-0.3	2.0	V
Supply Voltage, PLL	XVDD	-0.3	2.0	V
Supply Voltage, GPIO and data bus	IOVDD	-0.3	3.6	V
Input pin voltage: GPIO and data bus	V_{IO}	-0.3	IOVDD+1.0	V

Table 15. Absolute Maximum Ratings

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Temperature	T_A	-40		+85	°C
Digital supply voltage	DVDD	1.62	1.8	1.98	V
Supply voltage, PLL; same as DVDD	XVDD	1.62	1.8	1.98	V
I/O supply voltage; either 1.8V or 3V	IOVDD	1.62 2.7	1.8 3.0	1.98 3.3	V

Table 16. Operating Temperature and Voltage Range

Operation of the product at -40°C is assured with ATE guard banded conditions at room temperature test point. Updates are done to these limits as needed and in accordance with the u-Nav policy of change notification.

Note that IOVDD is either 1.8V or 3V. Operation outside of the 1.8 or 3V ranges is not supported. All data bus and GPIO pins will operate using the same IOVDD supply. Mixed I/O voltage levels is not supported.

DC Operating Characteristics

Item	Symbol	Test conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH}	IOVDD=3.0V or 1.8V	0.7 x IOVDD		IOVDD+1.0	V
Input low voltage	V_{IL}	IOVDD=3.0V or 1.8V	-0.3		0.3 x IOVDD	V
Output high voltage	V_{OH}	I_{OH} = -1 mA, IOVDD=3.0V or 1.8V	0.8 x IOVDD		IOVDD	V
Output low voltage	V_{OL}	I_{OL} = +1 mA, IOVDD=3.0V or 1.8V	0		0.2 * IOVDD	V
Input leakage current	I_{LI}	All Digital Pins	-10	+/- 1	+10	uA
Pull-up pull-down	R_{PU} R_{PD}	Pin Configured Appropriately	66K 38K	74K 50K	93K 79K	Ohm
Keeper resistance	R_{KP}	Pin Configured Appropriately		10K		Ohm

Table 17. DC Operating Characteristics of Digital Signals

DVDD core current *ICC* (includes XVDD) is tabulated below with typical values for an ambient temperature of 25°C. Maximum values are applicable over the full temperature range. ICC sleep current is dependent on IOVDD voltage. Functional blocks have been grouped together and correspond to continuous operating conditions. In real application, these blocks are turned on and off; therefore, many values below like Search Engine ICC correspond to peak current. Average core current is determined by software algorithm almost always yielding substantially lower average current consumption.

Item	Conditions	Min	Typ	Max	Unit
ICC, Correlator	1 Channel		3.7	8.0	mA
	8 Channels		5.3	10	mA
	12 Channels		6.2	11	mA
ICC, Search Engine	Search all four bins		10	15	mA
ICC, Sleep	IOVDD @ 1.8V IOVDD @ 3.0V		3 4	18 45	uA
ICC, VS_DSP Active	Looping on common instructions		6.4	12	mA
ICC, VS_DSP Idle	Halt instruction		1.8	3.5	mA
ICC, PLL			0.5	1.0	mA
ICC, other peripherals	All other peripheral blocks lumped together, excluding I/O current		1.0	2.0	mA

Table 18. Current Consumption by Functional Block

AC Operating Characteristics

Item	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}			3	pF
Output load capacitance	C_L			20	pF
Clock frequency, MCLK	f_C		16.3676		MHz
Clock period, MCLK	t_C		61		nS
Clock duty cycle, MCLK	t_{DUTY}	45	50	55	%

Table 19. AC Operating Characteristics of Digital Signals

Note that the clock period of 61 ns clock cycle is approximate and related to a frequency plan normally encountered with a uN8021C with MCLK of 16.3676MHz.

External Bus Timing

The external bus timing diagram follows. Note that the chip select signals have the same timing requirements as the address signals.

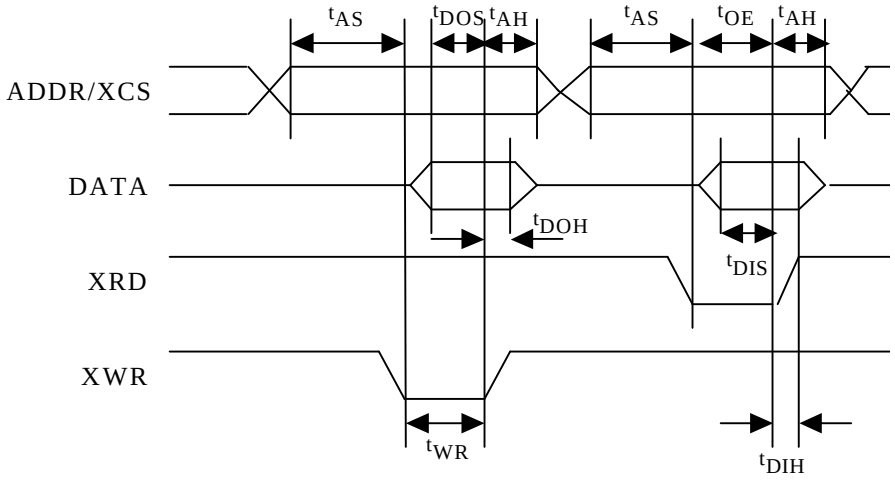


Figure 12. External bus timing diagram

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	4	7.5		nS
Address hold time	t_{AH}	15		30	nS
Write signal pulse width	T_{WR}	25		35	nS
Read signal pulse width	T_{RD}	25		35	nS
Data output setup time	T_{DOS}	5	8		nS
Data output hold time	T_{DOH}	10	21	25	nS
Data input setup time	t_{DIS}	1		7	nS
Data input hold time	t_{DIH}	2			nS

Table 20. External Bus Timing

External bus timing specifications in table 20 are given under 60pF load conditions.

Reset pin

The reset pin XRESET in the uN8130 implements a Schmitt trigger Reset level and timing is indicated below:

Item	Symbol	Min	Typ	Max	Unit
XRESET hold time	t_{XRH}	1000			nS
XRESET pulse width	t_{XRI}	1000			nS
Low-to-High	V_{LTH}	1.49	1.53	1.58	V
High-to-Low	V_{HTL}	1.26	1.29	1.32	V

Table 21. Reset Level and Timing

XRESET minimum time should be long enough to insure that one full RTC clock cycle occurs. For RTC frequency of 32768Hz, XRESET assertion should be greater than 2*31 microseconds in duration to insure a full RTC cycle is observed. In a complete system, other factors apply as described in the applications note section.

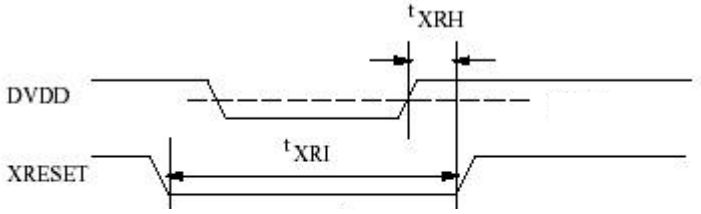


Figure 13. XRESET timing diagram

Application Notes

Power Sequencing

When using 3V I/O, insure that core voltage DVDD rises to 1.8V with or before IOVDD. Applying IOVDD without DVDD will cause improper internal biasing and a large current potentially damaging the device.

RTC and Reset

Typical RTC oscillator start-up at room temperature is less than 100uS, but it may become much longer at lower temperature. Typical TCXO start-up time may be 700uS. Since MCLK is sourced by the TCXO through the front-end RFIC, XRESET assertion should be long enough to insure stable MCLK. In practice, power-on XRESET assertion should be effectively be greater than 10mS. Note that RTC oscillation is not required for the device to reset; however, any sleep and wake-up modes require RTC for sequencing.

Programming Information

Refer to the *uN8130 Users Manual* for detailed information on register definition and programming information. Refer to the *uN8130 Errata List* for the latest information on device functional errata.

For further information, please contact:

Sales:

US.Sales@unav-micro.com
Europe.Sales@unav-micro.com
Korean.Sales@unav-micro.com
Japan.Sales@unav-micro.com
SoutheastASIA.Sales@unav-micro.com
Australia.Sales@unav-micro.com
NewZealand.Sales@unav-micro.com
India.Sales@unav-micro.com
China.Sales@unav-micro.com

Technical Support:

Technicalsupport.asia@unav-micro.com
TechnicalSupport.US@unav-micro.com
TechnicalSupport.Europe@unav-micro.com

Corporate Office:

u-Nav Microelectronics Corporate Headquarters
8 Hughes Irvine, Ca. 92618
Phone: +1 (949) 453-2727

Marketing:

Marketing@unav-mico.com

Website:

http://www.unav-micro.com/